REMARKS

In the Office Action, the Examiner reviewed claims 1-12 of the above-identified US Patent Application, with the result that claim 7 was objected to and all of the claims rejected under 35 USC §103. In response, Applicants have amended the claims as set forth above. More particularly:

The specification and independent claim 8 have been amended to clarify that the regions 32, 34, and 40 of the oxide layers 16 and 18 beneath the field oxide 42 are also removed prior to mating the cap wafer 10 with a device wafer. Support for these amendments can be found in Applicants' Figures 5, 6, and 7.[2]

Independent claim 8 has been further amended to clarify that multiple MEMS device packages 64 are produced with the method (which finds support in paragraph [0020] of the specification), to specify that the claimed method comprises "single wafer patterning steps" and "batch processing steps" that are performed on a cap wafer (10) and that all single wafer patterning steps performed on the cap wafer (10) precede the batch processing steps (which finds support in the second sentences of paragraphs [0008] and [0021] of the

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[2] According to MPEP §2163 II.A.3(a), "drawings alone may provide a 'written description' of an invention as required by [35 USC §112, first paragraph]," and "[i]n those instances where a visual representation can flesh out words, drawings may be used in the same manner and with the same limitations as the specification." (Citations omitted).

specification). The steps of the method are then grouped as appropriate as one of the "single wafer patterning steps" or one of the "batch processing steps."

Claim 8 and its dependent claims have been amended to provide consistent use of the term "cap wafer."

Claims 1 through 7 have been canceled without prejudice to Applicants in order to reduce and simplify the issues remaining in the examination of Applicants' application.

Applicants believe that the above amendments do not present new matter. Favorable reconsideration and allowance of remaining claims 8-12 are respectfully requested in view of the above amendments and the following remarks.

Objection to the Claims

The objection to claim 7 has been overcome by its cancellation.

Rejections under 35 USC §103

Remaining independent claim 8 and its dependent claims 9-12 were rejected under 35 USC §103(a) on the following grounds:

Claims 8, 9, and 11 were rejected as being unpatentable over U.S.

Patent No. 6,723,250 to Schaefer et al. (Schaefer) in view of U.S. Patent No. 6,913,701 to Moon et al. (Moon) and U.S. Patent No. 6,845,664 to Okojie;

Claim 10 was rejected as being unpatentable over Schaeffer, Moon, and Okojie as applied to its parent claim 8, and in further view of an excerpt from Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, 2000 (Wolf); and

Claim 12 was rejected as being unpatentable over Schaeffer, Moon, and Okojie as applied to its parent claim 8, and in further view of Applicants' admitted prior art (APA).

Applicants respectfully request reconsideration of these rejections in view of the claims as amended and the following comments.

Under each of the §103 rejections, Schaeffer was applied for teaching all of the limitations of the rejected claims except:

(1) Applicants' first and second oxide layers (16,18) over which the masking layers (20,22) are deposited and on which the oxide mask (42) is grown;

(2) the cap wafer (10) produced by Applicants' method, which is formed to have through-holes (48) and recesses (50) that are then aligned with bond pads (62) and micromachined elements (58) of a device wafer, followed by bonding the cap wafer (10) to the device wafer and then singulating individual device packages (62) from the resulting wafer stack;

(3) silicon dioxide as the "oxide" of the oxide mask (42); and

(4) the presence of defects in the masking layers (20,22).

Moon, Okojie, Wolf, and the APA were then applied as teaching limitations (1), (2), (3), and (4), respectively. However, Applicants believe none of the references disclose or suggest the additional limitations now recited in independent claim 8, namely, that all "single wafer patterning steps" precede "batch processing steps," the last of the former being the growth of an oxide mask (42) on exposed regions (32,34,40) of oxide layers (16,18). Furthermore, Applicants believe that none of the references disclose or suggest removing the oxide layers (16,18) along with the oxide mask (42). Applicants therefore respectfully request withdrawal of the rejections to remaining claims 8-12 under 35 USC §103(a).

Closing

In view of the above, Applicants respectfully request that their patent application be given favorable reconsideration.

Should the Examiner have any questions with respect to any matter now of record, Applicants' representative may be reached at (219) 462-4999.

Respectfully submitted,

By Domenica N S Hartman
Domenica N.S. Hartman
Reg. No. 32,701

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Hartman & Hartman, P.C.
Valparaiso, Indiana 46383
TEL.: (219) 462-4999
FAX: (219) 464-1166